	Application No.	Applicant(s)
Notice of Allowability	10/711,484 Examiner	MONAGHAN ET AL. Art Unit
	Cxammer	Art onlic
	Remmon R. Fordé	2826
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to 2/11/2005.		
2. The allowed claim(s) is/are <u>1-20</u> .	0.11	MATHAN J. PLYNN
3. \boxtimes The drawings filed on <u>21 September 2004</u> are accepted by	ne examiner	PERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800
4.		
 Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date 9/21/2004 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material 	6. Interview Summary Paper No./Mail Da' 08), 7. Examiner's Amendr	te

Application/Control Number: 10/711,484

Art Unit: 2826

DETAILED ACTION

Election Response

The Examiner hereby acknowledges Applicant's election with traverse of claims 1-14 in correspondence dated 2/11/2005. However, after further consideration the Examiner hereby withdraws the previous restriction requirement and will examine all pending claims 1-20.

Reasons For Allowance

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 1, 5 and 15 recite a semiconductor structure and a halo implant method for producing said semiconductor structure wherein the halo implant method includes the specific method steps of: providing first and second semiconductor structures formed on a same semiconductor substrate, wherein the first semiconductor structure comprises a first gate region and a first and second semiconductor regions, wherein the first gate region is oriented in a first direction, wherein the second semiconductor structure comprises a second gate region and a third and fourth semiconductor regions, wherein the second gate region is oriented in a second direction, wherein the first and second directions are essentially parallel to a top surface of the semiconductor substrate and are not parallel to each other; and halo-implanting the first, second, third,

Application/Control Number: 10/711,484

Art Unit: 2826

and fourth semiconductor regions in a third projected direction, wherein the third projected direction is essentially a bisector direction of the first and second directions. The abovementioned specific method steps and the resultant semiconductor structure are neither anticipated by nor obvious over the prior art of record. Likewise, claims 2-4, 6-14 and 16-20 are also allowable as being dependent upon allowable claims 1, 5, and 15 respectively.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Relevant Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rengarajan, Wang et al., Feudel et al. and Nowak et al. each disclose semiconductor devices processed with the aid of the halo implanting method. Application/Control Number: 10/711,484

Art Unit: 2826

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Remmon R. Fordé whose telephone number is (571) 272-1916. The examiner can normally be reached on Monday-Thursday (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Remmon R. Fordé